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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,396	10/29/2003	Kyong Seok Kim	041501-5582	6824

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MORGAN LEWIS & BOCKIUS LLP  
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WASHINGTON, DC 20004

EXAMINER
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CHUNG, DAVID Y

ART UNIT	PAPER NUMBER
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2871

MAIL DATE	DELIVERY MODE
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05/02/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

**Application No.**

10/695,396

**Applicant(s)**

KIM ET AL.

**Examiner**

David Y. Chung

**Art Unit**

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) 18-28 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-17 and 29 is/are allowed.
- 6) ☒ Claim(s) 30-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>23 October 2006</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 1. Claims 30, 31, 33 and 34 rejected under 35 U.S.C. 102(e) as being anticipated by Tsumura et al. (U.S. 6,704,066).**

As to claim 30, Tsumura discloses an in plane switching type liquid crystal display device in figures 4-6. Note the gate lines 201, data lines 202, pixel electrodes 210, common lines 209, and common electrodes 210. Figure 16 shows the driving sequence. Note the common voltage  $V_{scom}$  having a high level and low level. The data voltage  $V_{sd1}$  for the negative polarity display is supplied corresponding to the high level common voltage  $V_{scom}$ , and the data voltage for positive polarity display is supplied corresponding to the low level common voltage. See column 12, lines 32-57.

As to claim 31, Tsumura discloses a plurality of data lines 202 and gate lines 201 crossing each other in figures 4-6. A plurality of storage lines 209 are formed between

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the gate lines. First and second common voltages are alternately applied as shown in figure 16. Because a thin film transistor is connected to each gate line and each data line, a plurality of first thin film transistors and a plurality of second thin film transistors as claimed can be construed as being disclosed in figures 4-6. Each of the pixel electrodes is connected to the drain of one of the thin film transistors. The common electrodes 210 are connected to the storage lines 209.

As to claims 33 and 34, figure 16 shows high and low common voltages are alternately supplied to the storage line when a frame is changed. Figure 16 also shows that the alternation of the common voltage is synchronized with the gate pulse applied to each of the various gate lines.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**2. Claim 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura et al. (U.S. 6,704,066) in view of Moon et al. (U.S. 2002/0044246).**

Tsumura does not disclose a dummy line disposed along lowermost or uppermost portion in parallel with the gate lines. Moon discloses a dummy line 138 shown in figure 6. A portion of this line is parallel to the gate lines. Moon teaches that by providing this line, deterioration of the liquid crystal caused by a direct current voltage in the prior art can be prevented. See paragraph 0040. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a dummy line as claimed in order to prevent deterioration in the liquid crystal.

**3. Claim 32 rejected under 35 U.S.C. 103(a) as being unpatentable over Tsumura et al. (U.S. 6,704,066).**

Tsumura does not disclose a plurality of storage capacitors between the storage lines and liquid crystal capacitors. However, it was well known and obvious to form storage capacitors in order to improve the ability of the pixel electrode to hold the video signal, and thereby improve the display. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a storage capacitor in order to improve the ability of the pixel electrode to hold the video signal.

***Allowable Subject Matter***

Claims 1-17 and 29 allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record did not teach or suggest that the thin film transistors are

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formed at crossing points of the gate and data lines to be alternately positioned along the lower and upper side pixel regions adjacent to corresponding gate lines.

### ***Response to Arguments***

Applicant's arguments with respect to claims 30-35 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Y. Chung whose telephone number is (571) 272-2288. The examiner can normally be reached Monday thru Friday from 8:30 am to 5:00 pm. If successive attempts to contact the examiner are unsuccessful, the examiner's supervisor David C. Nelms can be reached at (571) 272-1787.

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800